IN THE CLAIMS:

Please amend claim 1 as shown in the complete list of claims that is presented below.

1. (previously presented) A digital filter circuit comprising:

a first RAM that stores sequentially input data having a first sampling period and sequentially outputs the data stored in the first RAM;

a second RAM that stores sequentially input data having a second sampling period sequentially outputs the data stored in the second RAM;

a first register that stores the data sequentially outputted from the first RAM <u>and</u> sequentially outputs the data stored in the first register;

a second register that stores the data sequentially outputted from the second RAM and sequentially outputs the data stored in the second register;

a cumulative arithmetic unit that computes the data outputted from the first [[RAM]] <u>register</u> and the second [[RAM]] <u>register</u>; and

a selector that alternately outputs the data outputted from the first register and the second register to the cumulative arithmetic unit.

2. (previously presented) A digital filter circuit according to claim 1, wherein the data having the first sampling frequency or the data having the second sampling frequency is caused to partly disappear by overwriting new data on the data within the first register or the second register.

3. (previously presented) A digital filter circuit according to claim 1, wherein the data computed by the cumulative arithmetic unit is fed back to the first register or the second register.

4. (original) A digital filter circuit according to claim 1, wherein the selector is operated to mix the data outputted from the first register or the second register with data outputted from the other register.

5. (previously presented) A digital filter circuit according to claim 1, wherein the digital filter circuit also has a mode in which the data having the first sampling period is directly inputted to the first register without being stored in the first RAM.

6. (original) A digital filter circuit according to claim 1, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.

7. (previously presented) A data processing method comprising the steps of:

sequentially inputting data having a first sampling period to a first RAM and storing the data having the first sampling period in the first RAM, wherein the data having a first sampling period is digitized first audio data;

sequentially inputting data having a second sampling period to a second RAM and storing the data having the second sampling period in the second RAM, wherein the data having a second sampling period is digitized second audio data;

sequentially outputting data sent from the first RAM to a first register and storing data sent from the first RAM in the first register;

sequentially outputting data sent from the second RAM to a second register and storing the data sent from the second RAM in the second register;

alternately outputting data from sent the first register and the second register to a cumulative arithmetic unit; and

computing the data outputted to the cumulative arithmetic unit so as to output some of the digitized first and second audio data from the cumulative arithmetic unit to thereby provide first and second audio data in compressed form.

8. (original) A data processing method according to claim 7, further comprising the step of causing the data having the first sampling frequency or the data having the second sampling frequency to partly disappear by overwriting new data on the data within the first register or the second register.

9. (original) A data processing method according to claim 7, further comprising the step of feeding back the data computed by the cumulative arithmetic unit to the first register or the second register.

10. (original) A data processing method according to claim 7, further comprising the step of mixing the data outputted from the first register or the second register with data outputted from the other register.

11. (previously presented) A data processing method according to claim 7, wherein the method includes a mode in which the data having the first sampling period in input directly to the first register without being stored in the first RAM.

12. (original) A data processing method according to claim 7, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.

13. (previously presented) A digital filter circuit according to claim 1, wherein the data having a first sampling period is digitized first audio data, wherein the data having a second sampling period is digitized second audio data, and wherein the cumulative arithmetic unit outputs some of the digitized first and second audio data to thereby provide first and second audio data in compressed form.